

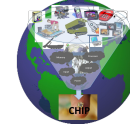


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IIT Hyderabad



**Chips to Startup
Programme**
An initiative by Ministry of Electronic
and IT, Government of India

SYNOPSYS[®]
Silicon to Software™



VLSI System Design

Cloud based Analog IC Design Hackathon

This is to certify that

Ruchit Chudasama

from
IIT Gandhinagar

has designed the circuit

HIGH SPEED LOW VOLTAGE CMOS FULL ADDER VLSI DESIGN

using Synopsys Custom Compiler Platform

She/He has performed an ~~Outstanding/Excellent/~~**Very Good**/~~Good~~ work.

This program was conducted between 15 February - 1 March 2022 as an initiative of IIT Hyderabad, which has been sponsored by Synopsys in association with VLSI System Design (VSD) Pvt.

Dr Ashudeb Dutta
Program Co-Ordinator, IIT Hyderabad

Dr B Umashankar
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