

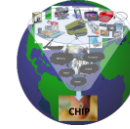


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IIT Hyderabad



**Chips to Startup
Programme**
An initiative by Ministry of Electronic
and IT, Government of India

SYNOPSYS[®]
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VLSI System Design

Cloud based Analog IC Design Hackathon

This is to certify that
Mohd Abdul Muqeem Nawaz

from

HCL Technologies

has designed the circuit

*Design of SRAM Cell Using Hybrid VLSI Techniques for Low Leakage and High Speed in
Embedded Memories*

using Synopsys Custom Compiler Platform

She/He has performed an ~~Outstanding/Excellent/~~**Very Good**/~~Good~~ work.

This program was conducted between 15 February - 1 March 2022 as an initiative of IIT Hyderabad, which has been sponsored by Synopsys in association with VLSI System Design (VSD) Pvt.

Dr Ashudeb Dutta
Program Co-Ordinator, IIT Hyderabad

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