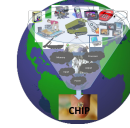




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IIT Hyderabad



**SYNOPSYS**<sup>®</sup>  
Silicon to Software™



VLSI System Design

# Cloud based Analog IC Design Hackathon

This is to certify that

*Bharat Suthar*

from

*Defence Institute of Advanced Technology, Pune*

has designed the circuit

*Full Adder Using CMOS Technology*

using Synopsys Custom Compiler Platform

She/He has performed an ~~Outstanding/Excellent/~~**Very Good**/~~Good~~ work.

This program was conducted between 15 February - 1 March 2022 as an initiative of IIT Hyderabad, which has been sponsored by Synopsys in association with VLSI System Design (VSD) Pvt.

**Dr Ashudeb Dutta**  
Program Co-Ordinator, IIT Hyderabad

**Dr B Umashankar**  
Chair CCE, IIT Hyderabad