



ಐಐಟಿ ಹೈದರಾಬಾದ್
आई आई टी हैदराबाद
IIT Hyderabad



**Chips to Startup
Programme**
An initiative by Ministry of Electronic
and IT, Government of India

SYNOPSYS[®]
Silicon to Software[™]



VLSI System Design

Cloud based Analog IC Design Hackathon

This is to certify that

Jeyanthi M

from

Thiagarajar College of Engineering

has designed the circuit

Implementation of CMOS based 1-bit Magnitude Comparator

using Synopsys Custom Compiler Platform

She/He has performed an ~~Outstanding/Excellent/Very Good~~ **Good** work.

This program was conducted between 15 February - 1 March 2022 as an initiative of IIT Hyderabad, which has been sponsored by Synopsys in association with VLSI System Design (VSD) Pvt.

Dr Ashudeb Dutta
Program Co-Ordinator, IIT Hyderabad

Dr B Umashankar
Chair CCE, IIT Hyderabad