National level Cloud based Analog IC Design Hackathon Statistics

https://hackathoniith.in

To push the Indian Govt initiative, **Chips to Start-up** (C2S) which aims to propel innovation, build domestic capacities to ensure hardware sovereignty, and build a Semiconductor Ecosystem Electrical Engineering department of **IIT Hyderabad** had conducted an "India`s first **Cloud based Analog IC Design Hackathon**" in collaboration with **Synopsys** India & **VLSI System Design** Corp. This event had provided participants a hands on Integrated circuit design experience with commercial Industry grade EDA tools. The entire hackathon had conducted on cloud platform with no-human-in-loop apart from doubt solving. The program has started on 15 February 2022 and closed on 8th March 2022.

Total 2444 had Registered from 24 countries of various universities across the globe.

Registration from foreign countries like (USA, Australia, Canada, Germany, Ireland, Netherland, Sweden, Switzerland, Japan, Taiwan) (Brasil, Colombia, Ecuador, Togo, Tunisia, Turkey, UAE, Egypt, Iraq, Israel, Philippines) (Bangladesh, Pakistan, Srilanka)

Total foreign participants: 58

Total working professionals: 548

Participants from (all IITs, NITs, Central universities, CFTIs, IIITs, almost all technical universities of India), (Arizona state univ, Columbia univ, Imperial clg of London, Lund univ, University of Michigan, Ottawa, FLorida and so on)

Participants form organizations like ISRO, SCL, CDAC, Intel, TI, Xilinx, NXP, Infineon, Broadcom, AMD, Accenture, AIML, Cognizant, TCS, Infosys, HCL, Hyundai, Mind Tree, Tech Mahindra, L&T, Mediatek, Microchip, HP and others

Literature review submitted by 481 participants
All 481 participants along with a volunteer team had used the software

Cloud server access provided to 481 participants on 20th Feb 2022
No of cloud servers used: 20 Client systems & 1 License server
Cloud servers terminated on 2nd March 2022 (10+1 days)

Final design report submitted by 246 nos out of 481 tool users on 1st March 2022

Other participants had used the tool but were unable to complete the design on time. All designs have been listed in a permanent web server, which can be accessed at https://hackathoniith.in

Participants from IISC, IIT Bombay, IIT Kgp, IIT BHU, IIT Delhi, IIT Tirpati, IIT Dharwad, IIT Varanasi, IIT Gandhi nagar, IIT Jammu, Indian institute of space technology, Institute of radio physics, almost all NITs, IIITs and many technical universities of all states of India

Including foreign students form Columbia univ, Cambridge university from USA & Philippines

Professionals from Analog devices, CDAC, HCL, NXP, HCL

Inauguration & Closing ceremony had been addressed by

Professor Shiv Govind Singh (Head of the department of Electrical engineering of IIT Hyderabad)

Professor Uma Shankar (Chair of Centre for Continuing Education (CCE) of IIT Hyderabad)

Professor Ashudeb Dutta (Professor in the department of Electrical engineering of IIT Hyderabad)

Dr Amit Acharyya (Associate professor in Department of Electrical Engineering of Indian Institute of Technology (IIT), Hyderabad

Mr Chinmaya Panda (Technical Officer (MicroElectronics & VLSI), department of Electrical engineering of IIT Hyderabad)

Mr Nishit Gupta (Scientist & Joint Director, in Microelectronics Development Division of Ministry of Electronics & Information Technology (Meity))

Mr Aveek Sarkar (Vice President - Synopsys Inc)

Mr Raja Subramaniam (Country Director at Synopsys India Pvt Ltd)

Mr Srinivas Macha (Inia Account management head, Synopsys)

Mr Patrick Haspel (Global university program, Synopsys)

Mr Kunal Ghosh (Founder of VLSI System Design (VSD)

Ms Anagha Ghosh (Founder of VLSI System Design (VSD)

Along with other winners and core team members.

The design hackathon had been planned from July 2021 and complete on 8th March 2022. Which took almost 7 months of time by a group of dedicated team members.

Before the start of the hackathon Mr Panda of IIT Hyderabad, Mr Kunal of VSD & Synopsys team had exactly calculated the resource requirements and tested tools vigorously with different versions of tools, compatibilities, OS version and possibilities of physical servers & cloud servers.

Finally 21 Cloud server had been created by Mr Chinmaya Panda & Mr Kunal along with software, licenses & remote connections to accommodate 500+ participants to do the design at a time without any major issues.

By considering various groups & categories of participants a web-based server access had been created, so every user had used the servers for 11 days using their favorite web browser like google chrome or Mozilla without installing any software.

A volunteer team had worked continuously to keep the servers up and to resolve the issues of participants. Several videos, documents had been created to facilitate the use of such massively complex software to be used by participants without even noticing all the odds. As

per Synopsys this was the first such successful & massive cloud-based EDA design hackathon in world.

Finally, we can say that India as well as world has experienced the possibilities of use of massively complicated EDA tool usage over cloud platform. It will create a new era in coming years when we go over cloud infrastructure for Integrated circuit designs instead of making discrete local infrastructure.

Closing ceremony Cloud based Analog IC Design Hackathon